facing away from said chip, said dielectric element having a hole encompassing said central contacts and an edge bounding said hole;

(c) a plurality of [central] terminals disposed on said dielectric element for interconnection to a substrate and overlying said chip front surface; and

(d) a plurality of central contact leads extending between at least some of said central contacts and at least some of said [central] terminals, each said central contact lead having a terminal end connected to one of said [central] terminals and a contact end [projecting across the edge bounding said hole] extending to one of said central contacts, said [central] terminals being movable with respect to said central contacts so as to compensate for thermal expansion of said chip.

B1

2 ~~62~~. (Amended) A chip assembly as claimed in claim ~~61~~ 1, wherein the terminal end of each said central contact lead is integrally formed with one of said [central] terminals.

4 ~~64~~. (Amended) A chip assembly as claimed in claim ~~61~~ 1, wherein said dielectric element includes a compliant layer of a low modulus material, said compliant layer being disposed beneath said [central] terminals.

B2

8 ~~68~~. (Amended) A chip assembly as claimed in claim ~~61~~ 1, wherein said dielectric element includes a sheet-like, electrically conductive grounding layer [disposed between said central terminals and said chip].

B3

9 ~~69~~. (Amended) A chip assembly as claimed in claim ~~61~~ 1, wherein some of said [central] terminals are disposed adjacent the edge bounding said hole.

10 ~~70~~. (Amended) A chip assembly as claimed in claim ~~61~~ 1, wherein said plurality of [central] terminals are disposed at said second surface of said dielectric element.